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EXAMINER	
PHAM, CHRYSTINE	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,567	CHOI ET AL.	
	Examiner	Art Unit	
	Chrystine Pham	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

TC

DETAILED ACTION

1. This action is responsive to amendment filed on February 23rd 2005. Claims 1, 4, 6, 7, 11-13, 15, 17, and 20 have been amended. Claims 21-23 are new claims. Claims 1-23 are presented for examination.

Response to Amendment

2. In view of the amendment made to claims 6 and 7 to refer to claim 5 instead of claim 1, rejection of the claims under 35 USC 112 second paragraph is hereby withdrawn.

Response to Arguments

3. Applicant's arguments filed February 23rd 2005 have been fully considered but they are not persuasive.

The Applicant essentially contends that "Mellor-Crummey does not teach or suggest processing the set of input information by comparing threads that may execute statements in a statement pair" (page 9-10). It is submitted that on page 132, right column, first paragraph under **section 3.2 Intraprocedural Strategy**, Mellor-Crummey explicitly states that "variable references to memory locations that are not accessed by more than one thread **do not need** data race instrumentation" (emphasis added). In the last paragraph before section 3.2, Mellor-Crummey discloses said variable references are part of a program statement. It is clear Mellor-Crummey only instruments variable references (i.e., statements in a statement pair) that are accessed by more than one thread (i.e., threads). That is to say, Mellor-Crummey only considers at least two variable references (i.e., statements in statement pair), each belongs to a separate thread, which access the same memory location. It is clear that [variable references from different] threads have to be compared in order to identify (i.e., determine) those [variable references] that may cause a data race during execution (see at least *data race, two or more accesses to same shared variable* page 129, left column, 1st paragraph under **section 1 Introduction;** *data dependence analysis, compile-time analysis, two variable references, same memory location* page 132, right

column, 2nd paragraph under **section 3.2 Intraprocedural Strategy**). In other word, it is inherent that Mellor-Crummey "compares threads that may execute statements in a statement pair", otherwise, it would be impossible to detect data race caused by multiple threads accessing the same memory location (via variable references or statements in a statement pair).

The Applicant further points to page 15, line 8 through page 18, line 12 of the specification, Fig.3, 4, and 6 as supposedly disclosing "explicitly tag each statement with the set of threads that may execute it and compare these sets of different statements to determine whether two statements can cause data race during execution". However, nowhere on page 15 through page 18, and no discussion of Figures 3, 4, or 6 describes this concept of "explicitly tagging a statement with a set of threads". Figure 3 simply illustrates the steps to determine a statement conflict set, which involves computing a node conflict set as recited in claim 10. Figure 4 illustrates the steps of identifying all reachable conflicting node pairs for each distinct pair of thread-root nodes, and identifying all reachable conflicting node pairs for each thread-root node as recited in claims 12-13. Figure 6 illustrates a program segment with two threads (i.e., multithreaded application) as recited in claim 1. Furthermore, comparing these sets of different statements (which are supposedly "tagged") "to determine whether two statements can cause data race during execution" is clearly anticipated by Mellor-Crummey as already established above.

The Applicant further claims that "static analysis may compare the sets of locks held by threads while executing statements in deciding whether the execution may cause a data race during execution" (page 10). It is noted that, the term "lock" is not mentioned anywhere in the specification, much less this concept of "comparing sets of locks" which the Applicant has added to new claim 22.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (page 11, 4th full paragraph), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to Applicant's argument that the references (i.e., Mellor-Crummey and Flanagan) do not include any motivation to urge the combination, it is submitted that the motivation for combining the reference, as cited in previous Office Action (in claim 14) is suggested by Flanagan (see Flanagan col.3:60-col.4:6).

4. In view of the fore going discussion, rejection of claims 1-13, 17-20 under 35 U.S.C. 102(b) and claims 14-16 under 35 U.S.C. 103(b) is considered proper and maintained.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 21-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement and the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention or to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 21 recites "tagging a statement with a set of threads" in line 3. This limitation is claimed by the Applicant to have been described in the specification on page 15, line 8 through page 18 line 12, Figures 3, 4, and 6. However, nowhere on page 15 through page 18, and no discussion of Figures 3, 4, or 6 describes how this concept of "tagging a statement with a set of threads", much less "explicitly tagging a statement with a set of threads". Figure 3 simply illustrates the steps to determine a statement conflict set, which involves computing a node conflict set as recited in claim 10. Figure 4 illustrates the steps of identifying all reachable conflicting node pairs for each distinct pair of thread-root nodes, and identifying all reachable conflicting node pairs for each thread-root node as recited in claims 12-13. Figure 6 illustrates a program segment with two threads (i.e., multithreaded application) as recited in claim 1. For compact prosecution of the claims, "tagging a statement with a set of threads" deemed inherent and thus equivalent to "comparing threads that may execute statements in a statement pair" as discussed above in the Response to Arguments section.

Claim 22 recites "comparing sets of locks held by threads" in line 3. Nowhere in the specification is the term "lock" mentioned, much less the description of "comparing sets of locks held by threads". Claim 22 is thus, withdrawn from further consideration.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-13, 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Mellor-Crummey (Compile-time Support for Efficient Data Race Detection in Shared-Memory Parallel Programs,

http://portal.acm.org/citation.cfm?id=171370&dl=GUIDE&coll=GUIDE&CFID=31826656&CFTOKEN=65552401), hereinafter, *Mellor-Crummey*.

Claim 1

Mellor-Crummey teaches a computer processing system and a computer program product (e.g., see page 130 left column last paragraph for *ParaScope* & associated text) and method for statically detecting a datarace in a multithreaded application (e.g., see Abstract; see page 129 right column 1st paragraph for *static analysis* & associated text; see page 130 left column last paragraph for *ParaScope* and *static program analysis* & associated text; see page 132 right column first paragraph under section 3.2 for *thread of control* & associated text), said method comprising:

- inputting a set of input information (stored in a storage medium) via an input interface (e.g., see page 130 right column 2nd paragraph under section 2 ParaScope under subsection 1 Local Analysis for *editors*, *summary information* & associated text; see page 130 right column 1st & 2nd paragraphs under section 2 ParaScope for *whole-program* and *procedures* & associated text);
- a processor receiving and processing the set of input information by comparing threads that may execute statements in a statement pair (i.e., tagging a statement with a set of threads that may execute said statement, and comparing sets of threads for said statements) (e.g., see page 130 right column 1st paragraph under section 2 ParaScope for *dependence analysis, interprocedural analyses* & associated text; *statement, variable references, intraprocedural strategy, thread, memory locations, data dependence analysis* page 132, right column); and
- computing and outputting, via an output interface, a statement conflict set that identifies the statement pairs whose execution instances definitely or potentially cause dataraces (e.g., see page 132 right column 2nd paragraph under section 3.2 Intraprocedural Strategy for *data dependence analysis*, *dependence graph*, and *dependence edge* & associated text), without executing the multithreaded application (e.g., see Abstract for *compile-time analysis*) .

Claim 2

The rejection of base claim 1 is incorporated. *Mellor-Crummey* further teaches wherein the processing comprises:

- selectively evaluating the input information (i.e., a given pair of reference expressions) with an IsPotentialDR relation (e.g., see page 129 right column 2nd paragraph 1st sentence for *two references*); and
- selectively evaluating the input information (i.e., a given pair of reference expressions) with an IsDefiniteDR relation (e.g., see page 129 right column 3rd paragraph 1st sentence for *feasible races*).

Claim 3

The rejection of base claim 2 is incorporated. *Mellor-Crummey* further teaches wherein, for a given pair of reference expressions, the IsPotentialDR relation comprises:

- determining whether the reference expressions might be executed by different threads (negation of DefSameThreadObj) (e.g., see page 132 left column 1st full paragraph 3rd bullet for *access history declarations* & associated text; see same column 1st & 2nd paragraphs under section 3.1 Basic Strategy for *parallel construct*, *procedure references* & associated text);
- determining whether the reference expressions might access the same field of the same object (e.g., see page 132 right column 2nd paragraph under section 3.2 Intraprocedural Strategy for *same memory location* & associated text); and
- determining whether the reference expressions might not be mutually synchronized (negation of DefSync) (e.g., see page 131 1st paragraph under section 3 Data Race Instrumentation for *synchronization*, *on-the-fly monitoring* & associated text; see page 130 left column 2nd paragraph for *on-the-fly techniques*, *unordered conflicting accesses* & associated text).

Claim 4

The rejection of base claim 2 is incorporated. *Mellor-Crummey* further teaches wherein, for a given pair of reference expressions, the IsDefiniteDR relation comprises:

- determining whether the reference expressions cannot be executed by the same thread (negation of PossSameThreadObj) (e.g., see page 132 right column 1st paragraph under section 3.2 Intraprocedural Strategy for *thread of control* & associated text);
- determining whether the reference expressions must access the same field of the same object (e.g., see page 132 right column 1st paragraph under section 3.2 Intraprocedural Strategy for *memory locations* & associated text);
- determining whether the reference expressions cannot be mutually synchronized (negation of PossSync) (e.g., see page 130 left column 2nd paragraph for *on-the-fly techniques*, *unordered conflicting accesses*, *feasible races* & associated text); and
- determining whether the reference expressions must execute (e.g., see page 130 left column last paragraph for *compile-time analysis* & associated text; see page 131 right column last paragraph 2nd bullet for *access check* & associated text).

Claim 5

The rejection of base claim 1 is incorporated. *Mellor-Crummey* further teaches wherein the set of input information comprises a multithreaded context graph (multithreaded context graphs) (i.e., meta-information relating to the multithreaded application) (e.g., see page 131 left column 1st paragraph under section 3 Data Race Instrumentation for *program modules*, *abstract syntax trees* & associated text).

Claim 6

The rejection of base claim 5 is incorporated. *Mellor-Crummey* further teaches wherein the multithreaded context graph comprises an interprocedural call graph having each of a

plurality of synchronized blocks (i.e., synchronized methods) as a separate node (e.g., see page 131 left column under subsection 2 Interprocedural Propagation for *call graph* & associated text; see page 131 1st paragraph under section Data Race Instrumentation for *program modules*, *synchronization events*, *synchronization traces* & associated text).

Claim 7

The rejection of base claim 5 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 8

The rejection of base claim 1 is incorporated. *Mellor-Crummey* further teaches performing dynamic datarace detection on the statement conflict set (e.g., see page 131 right column 1st paragraph under section 3 Data Race Instrumentation for *on-the-fly monitoring* & associated text).

Claim 9

The rejection of base claim 1 is incorporated. *Mellor-Crummey* further teaches performing escape analysis to identify statements that can access memory locations accessible by more than one thread (e.g., see page 132 right column 1st paragraph under section 3.2 Intraprocedural Strategy for *variable references* and *data race instrumentation* & associated text).

Claim 10

The rejection of base claim 1 is incorporated. *Mellor-Crummey* further teaches wherein the processing comprises:

- computing a node conflict set (e.g., see pages 132-133 2nd paragraph under section 3.2 Intraprocedural Strategy for *dependence graph*, *node* & associated text); and

- computing the statement conflict set by determining pairs of conflicting statements in the node conflict set (e.g., see pages 132-133 2nd paragraph under section 3.2 Intraprocedural Strategy for *dependence graph*, *dependence edge* & associated text).

Claim 11

The rejection of base claim 10 is incorporated. *Mellor-Crummey* further teaches wherein said computing the node conflict set comprises:

- initializing a synchronization object set for each of a plurality of multithreaded context graph node (e.g., see page 131 1st paragraph under section 3 Data Race Instrumentation for *augment Fortran ASTs*, *adding calls* & associated text).

Claim 12

The rejection of base claim 11 is incorporated. *Mellor-Crummey* further teaches wherein said computing the node conflict set further comprises: identifying all reachable conflicting node pairs for each thread-root node (e.g., see page 130 left column 2nd full paragraph for *on-the-fly* & associated text; see page 132 left column 1st paragraph 3rd bullet for *access history declarations* & associated text).

Claim 13

The rejection of base claim 12 is incorporated. *Mellor-Crummey* further teaches wherein the node conflict set computing further comprises:

- identifying all reachable conflicting node pairs for each distinct pair of thread-root nodes in the multithreaded context graph (e.g., see pages 132-133 1st – 4th paragraphs for *dependence graph*, *edge*, *data dependence* & associated text); and
- identifying all reachable conflicting node pairs for each thread-root node in the multithreaded context graphs that is invokeable by more than one thread (e.g., see

page 132 1st paragraph under section 3.2 Intraprocedural Strategy for *variable references, thread of control* & associated text).

Claims 17-19

Claims recite limitations, which have been addressed in claims 1, 5, 8, therefore, are rejected for the same reasons as cited in claims 1, 5, 8.

Claim 20

Claim recites a computer program product comprising a computer readable medium having computer code embodied therein for performing the method addressed in claim 1, therefore, is rejected for the same reasons as cited in claim 1.

Claim 21

The rejection of base claim 1 is incorporated. Claim recites limitations, which have been addressed in claim 1, therefore, is rejected for the same reasons cited in claim 1.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 14-16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Mellor-Crummey* in view of Flanagan et al. (US 6343371), hereinafter, *Flanagan et al.*.

Claim 14

The rejection of base claim 1 is incorporated. *Mellor-Crummey* further teaches wherein the input comprises meta-information relating to a multithreaded application (see claim 5). *Mellor-Crummey* does not expressly disclose [the application] written in an object-oriented programming language. However, *Flanagan et al.* teach a method of statically detecting data race in multithreaded application written in an object-oriented programming language (e.g., see Abstract; col.4:9-15). *Mellor-Crummey* and *Flanagan et al.* are analogous art because they are both directed to a method of statically detecting data races in computer programs. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Flanagan et al.* into that of *Mellor-Crummey* for the inclusion of an object-oriented program. And the motivation for doing so would have been to support non-finite state systems (i.e., dynamic object allocation).

Claim 15

The rejection of base claim 1 is incorporated. Claim recites limitations, which have been addressed in claims 5 and 14, therefore, is rejected for the same reasons as cited in claims 5 and 14.

Claim 16

The rejection of base claim 15 is incorporated. *Mellor-Crummey* further teaches wherein the input further comprises a plurality of bytecodes that collectively comprise the application (e.g., see page 130 left column last paragraph for *ParaScope, run-time monitoring* & associated text).

Claim 23

Claim recites a method for statically detecting a datarace condition recited in claims 1, 8-14, therefore, is rejected for the same reasons cited in claims 1, 6-14.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571-272-3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CP
May 28, 2005

WEI Y. ZHEN
PRIMARY EXAMINER